

PRELIMINARY

YVX-657

Voxtel Time-to-Digital Converter Board

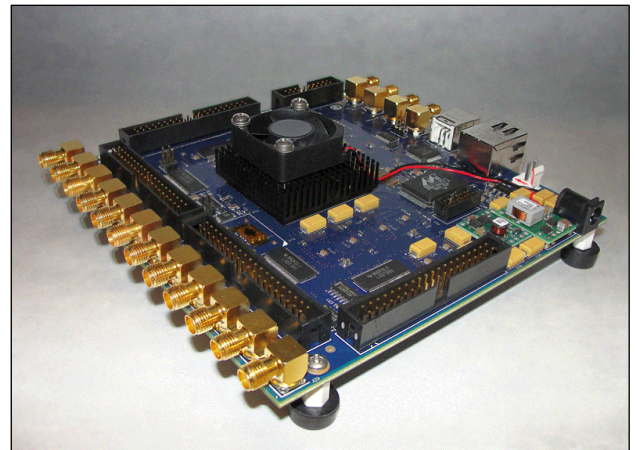
A compact, easy-to-use, plug-and-play 64-channel time-to-digital converter (TDC)

Summary of Features

- 8 CMOS channels (SMA connectors) or 64 LVDS channels (DIP connectors); 1 common CMOS reference input channel that can be used as a regular CMOS input channel
- One common start input for all channels
- Fully digital design
- <32 ps typical timing resolution
- 32-bit time stamps recorded on each channel
- Large internal memory buffer, with a minimum on-board storage capacity of 65,535 event time stamps per channel. (262,144 events per channel for 8-channel version)
- Two operating modes: free-running/continuous, gated
- Maximum input event rate of up to 12.5 million events/sec for each channel (>30 MHz on 8-channel board)
- Over-voltage protected inputs
- User-friendly software for Windows, support for user control of the software through a local host interface
- Statistical data processing
- Export of data files into other programs such as MS Excel
- Low-jitter and ultra-stable ovenized quartz crystal time base, or external clock input
- Gigabit Ethernet
- Single 5-V power supply required for operation
- Low power consumption (<20 W)

Applications

- LIDAR
- LADAR camera electronics
- Time-of-flight measurements
- Single photon counting
- Dynamic Light Scattering/Photon Correlation Spectroscopy
- High-energy physics experiments
- Dynamic testing of integrated circuits (ICs) and hard drives
- Evaluation of high-speed data transfer in telecommunications
- Quantum cryptography



The VX-657 is a single-start/multi-stop multi-channel time to digital converter (TDC) designed using state-of-the-art components, offering excellent performance and ease of use. The VX-657 records the difference between a reference time and pulses arriving on any of the 8 CMOS input channels or 64 LVDS channels, with <32 ps of timing jitter. For each channel, up to 262,144 32-bit time stamps can be recorded and stored on on-board memory before downloading to PC through gigabit Ethernet (GbE).

The TDC time base (master clock) consists of a low-phase-noise PLL with extremely low jitter and a highly stable, high-accuracy 20-MHz reference oven-controlled crystal oscillator (OCXO). Alternately, users can reference the board to an external 20-MHz source through an external clock input.

To initiate operation, the VX-657 TDC is first armed by a user-supplied 'TDC Enable' (start) pulse. A periodic hold signal ('Hold Enable') can be used to effect a gated operating mode. While the TDC Enable input is held high, each channel records the time of arrival of subsequent input events and stores the relevant data in local memory. The time of arrival of each input event is measured relative to the rising edge of the TDC Enable pulse; falling-edge detection may be used in the 8-channel TDC. Each input channel records pulse arrival time with a resolution of <32 ps.

The time stamps can be downloaded to PC through GbE using Voxtel's easy-to-use software. The Windows-based software provides a powerful GUI for setup, acquisition, data transfer, statistical calculations and data display. The software calculates and displays the arrival time of each event, accounting for delay (calibration) values on each of the channels; the user can select these delay values based on their measurement setup, accommodating typical measurement setups including cable delays, delays from the start of the laser trigger pulse to the light output pulse, etc. The calibration value for each channel is stored on an on-board EEPROM and recalled at TDC start-up. The software is designed to facilitate integration with the user's experimental needs.

Typical Specifications

Measurement range	13.3 ms
Timing resolution/Jitter	<32 ps
Time stamp	32 bits
Events per channel before transfer to host	262,144 (8 channels) / 65,535 (65 channels)
Pulse pair resolution	<35 ns (8 channels) / 75 ns (65 channels)
Maximum input count rate	25 MHz (8 channels) / 12.5 MHz (65 channels)
Minimum input pulse width	7.25 ns
Operating modes	Free-running mode or gated mode
Time base	Internal, highly stable oven-controlled crystal oscillator or external 20-MHz input through SMA connector
Differential non-linearity (DNL)	±1 LSB
Event input	8-channel TDC: 8 CMOS (SMA) + 1 reference channel (SMA) 64-channel TDC: 64 LVDS (four 2 × 20 IDC sockets) + 1 reference channel (SMA)
Other inputs (SMA)	<ul style="list-style-type: none"> • Common TDC Enable input • Hold input (inhibit input events) • Reference input • External clock input
Input levels	CMOS (4.6 V absolute maximum)
PC interface	Gigabit Ethernet (USB 2.0 available on request)
Software requirement	Windows XP or later
Power requirement	+5 V, 3 A (typical for board)
Board dimensions	5.5" × 5.5"

Inputs

1. TDC Enable: SMA connector, 50 Ω terminated, CMOS input (+3.3 V), protected to +4.6 V.

The TDC Enable signal starts the TDC operation and is required at all times.

2. Event Inputs:

- **8-channel TDC:** 8 SMA connectors, 50 Ω terminated, CMOS inputs (+3.3 V), protected to +4.6 V.

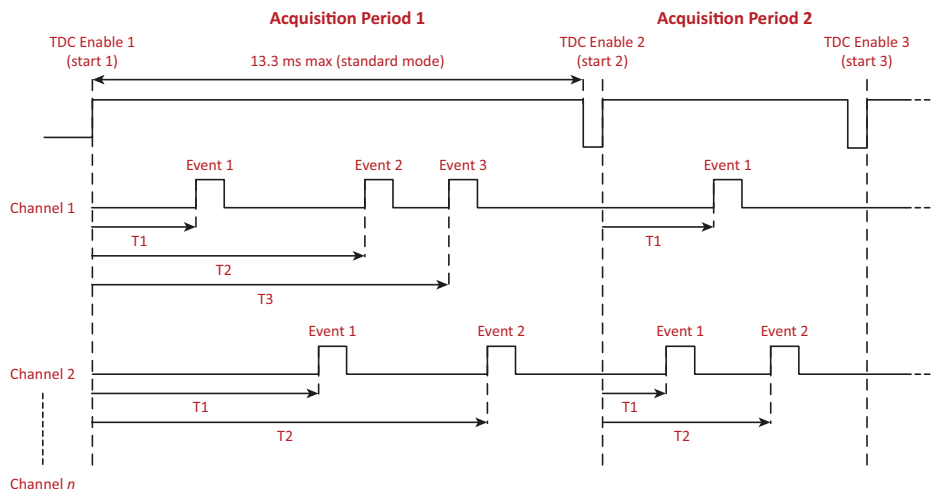
- **64-channel TDC:** Four 2 × 20 IDC sockets, 100 Ω terminated, 16 input channels on each socket.

3. TDC Hold: SMA connector, 50 Ω terminated, CMOS input (+3.3 V), protected to +4.6 V.

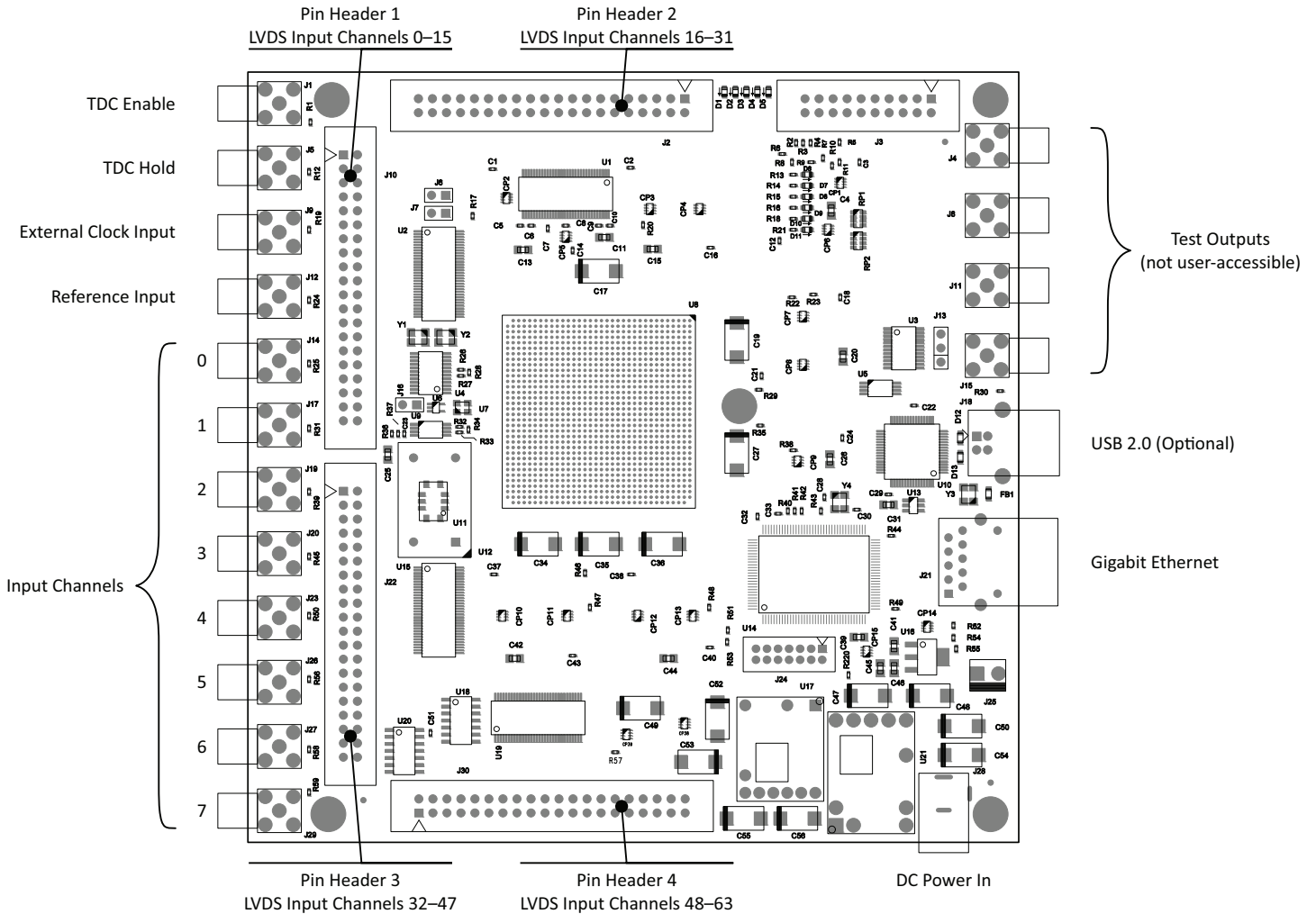
The TDC Hold signal is used to mask event input; when it is high, event inputs are not registered. Without any signal on this input, all event inputs are processed by the FPGA (free-running mode), while a periodic hold signal will produce a gated mode of operation.

4. Reference channel input: SMA connector, 50 Ω terminated, CMOS input (+3.3 V, protected to +4.6 V). This input provides flexibility for creative uses such as asserting the optical signal pulse from the laser, or can be used as an additional event input channel.

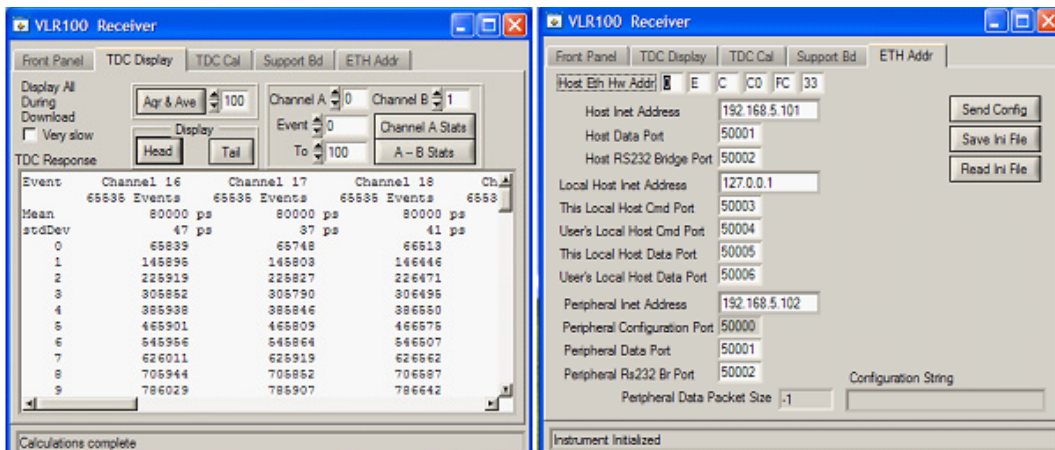
Output: The TDC data is downloaded to PC through GbE using easy-to-use GUI-based software.



Operating principle of Voxtel's common-start/multi-stop time-to-digital converter in standard mode. Following each acquisition period, data is downloaded from on-board memory to the host PC. Falling-edge detection is available on all 8 channels, or on selected channels.



TDC board layout.



Screenshots of the GUI for the TDC.